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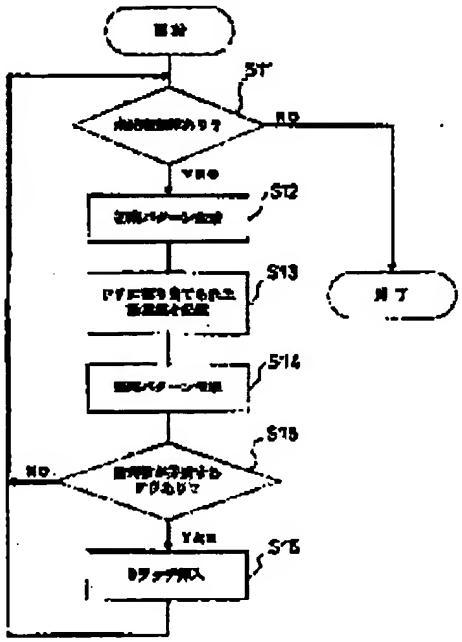
(54) INSPECTION FACILITATION DESIGN METHOD FOR ROUTE DELAY FAULT AND INSPECTION SYSTEM GENERATION METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an inspection facilitation design method for a route delay fault, which can obtain a high fault detection rate without considerably increasing area overhead.
SOLUTION: The unprocessed route delay fault which is given in an integrated circuit is selected (S11). An initial pattern is generated for the selected route delay fault (S12), and logic values which are set in respective scan flip flops are stored (S13). A transition pattern is generated for the selected route delay fault (S14). It is judged whether the scan flip flop where the logic value is contradicted between the initial pattern and the transition pattern exists or not (S15). A D latch is inserted into the output signal line of the scan flip flop whose logic value is contradicted (S16). The contradiction of the logic value is dissolved by the D latch and the inspection of the route delay fault becomes easy.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the inspection sequence generation method which generates the inspection sequence over the integrated circuit to which inspection easy-ization was performed by the inspection easy-ized design approach which makes inspection of path delay failure easy especially, and said inspection easy-ized design approach about the inspection easy-ized design approach and inspection sequence generation method of an integrated circuit.
[0002]
[Description of the Prior Art] The outstanding inspection easy-ized design approach and the outstanding inspection sequence generation method are demanded with improvement in the degree of integration of an integrated circuit. The needs of the inspection easy-ized design approach which makes inspection of path delay failure easy especially, and an inspection sequence generation method are increasing.
[0003] A thing typical as the inspection approach of path delay failure is the following three.
(1) Only the shift action of a scanning flip-flop generates an initial pattern and a transition pattern.
(2) The shift action of a scanning flip-flop generates an initial pattern, and normal operation generates a transition pattern after that.
(3) In addition to the approach of (1), use the scanning flip-flop cel of dedication which connected the D flip-flop to the output of a scanning flip-flop.
[0004] The inspection sequence generation method of the conventional path delay failure and the inspection easy-ized design approach are indicated by the bibliography of "Design-for-Testability for Path Delay Faults in Large Combinational Circuits Using Test-Points" (I. Pomeranz, S.M.Reddy, 1994, design automation conference) and this reference.
[0005]
[Problem(s) to be Solved by the Invention] However, there are the following problems in the inspection approach of the conventional path delay failure.
[0006] First, by the approach of (1), an initial pattern and a transition pattern are ungenerable with the shift action of a scanning flip-flop in many cases. Therefore, the detection ratio of path delay failure is bad.
[0007] Moreover, according to the approach of (2), although fault coverage generally improves compared with the approach of (1), when setting a logical value as a common scanning flip-flop by the initial pattern and the transition pattern, in this scanning flip-flop, conflict may arise in a logical value, and generation of an initial pattern or a transition pattern may go wrong. In such a case, fault coverage falls on the contrary.
[0008] Furthermore, by the approach of (3), since a scanning inn is performed so that a transition pattern may be made to hold to the D flip-flop in a scanning flip-flop cel, fault coverage improves compared with the approach of of (1) and (2). However, in order to use the scanning flip-flop cel of dedication, the area overhead of an integrated circuit increases sharply. Moreover, since two flip-flops are contained in one scanning flip-flop cel, the number of test patterns required for a scanning inn doubles compared with the approach of of (1) or (2), and the number of test patterns increases.
[0009] Let it be a technical problem to offer the inspection easy-ized design approach and inspection sequence generation method for path delay failure which can obtain high fault coverage, without causing large increase of the number of test patterns which the area overhead of an integrated circuit and inspection take this invention in view of the aforementioned problem.
[0010]
[Means for Solving the Problem] In order to solve the aforementioned technical problem, the solution means which invention of claim 1 provided As the inspection easy-ized design approach of path delay failure of performing a design change so that inspection of path delay failure may become easy to the

given integrated circuit When the scanning flip-flop to which the logical value to which the logical value was set up and set [in / both / the initial pattern and transition pattern which were generated for inspection] is contradictory with an initial pattern and a transition pattern exists in an integrated-circuit circuit, It is what arranges the value maintenance component which has the function to once hold the inputted data according to the directions from the outside in the location which can hold the output data of the scanning flip-flop concerned in said integrated circuit. By this Since conflict of the logical value of said scanning flip-flop is canceled and failure in generation of an initial pattern and a transition pattern can be prevented, high fault coverage can be obtained.

[0011] The solution means which invention of claim 2 provided materializes invention of claim 1. As opposed to the integrated circuit by which the full scan design was carried out While making an external input terminal or the data output terminal of a scanning flip-flop into the starting point, an external output terminal or the data input terminal in the normal mode of a scanning flip-flop is made into a terminal point, and it can set to the signal path of the arbitration constituted from the starting point by only the combinational circuit to the terminal point. As the inspection easy-ized design approach of path delay failure of performing a design change so that the existence of path delay failure which takes the time amount more than a clock period for the signal outputted from the starting point to arrive at a terminal point can be inspected easily If the signal outputted from the starting point of a signal path starts, the signal outputted from the starting point of a signal path falls, it starts, path delay failure which is a signal is considered as delay failure and the path delay failure which is a signal is [it falls and] delay failure By path delay failure to be examined starting, when it is delay failure So that a logical value "1" may be set as the starting point of said signal path when it is falling delay failure and said signal path may be activated further, while setting a logical value "0" as the starting point of a signal path when path delay failure was assumed By setting a logical value as external input terminals other than the starting point of said signal path, or the data output terminal of a scanning flip-flop The 1st processing which generates an initial pattern, and the 2nd processing which memorizes respectively the logical value concerned of each scanning flip-flop with which the logical value was set as the data output terminal in the initial pattern generated by said 1st processing, By said path delay failure to be examined starting, when it is delay failure While setting a logical value "1" as the starting point of said signal path, when it is falling delay failure, a logical value "0" is set as the starting point of said signal path. When the starting point of said signal path is the data output terminal of a scanning flip-flop A logical value is set as an external input terminal or the data output terminal of a scanning flip-flop so that it may be in agreement with the logical value to which the input data in the normal mode of this scanning flip-flop was set. Furthermore, so that it may be respectively in agreement with the logical value the input data in the normal mode of scanning flip-flops other than the starting point of said signal path when the logical value was set as the data output terminal in said initial pattern was remembered to be by said 2nd processing By setting a logical value as an external input terminal or the data output terminal of a scanning flip-flop It judges whether the scanning flip-flop which has the data output terminal for which the logical value to which the logical value was set up and set [in / both / said initial pattern and the transition pattern] is contradictory to the 3rd processing which generates a transition pattern with an initial pattern and a transition pattern exists in an integrated circuit. When it exists, it considers as a configuration equipped with the 4th processing which arranges the value maintenance component which has the function to once hold the inputted data with the directions from the outside in the location which can hold the output data of the scanning flip-flop concerned in said integrated circuit.

[0012] The initial pattern for inspecting the existence of path delay failure first by invention of claim 2 to the integrated circuit given by 1st processing is generated. The logical value set as the data output terminal of each scanning flip-flop in the initial pattern by 2nd processing is memorized. Next, the transition pattern for inspecting the existence of path delay failure to the given integrated circuit by 3rd processing is generated. When it is judged whether the scanning flip-flop with which the logical value set as the data output terminal is contradictory exists and it exists by the initial pattern and the transition pattern by 4th processing, the value maintenance component which has the function to once hold the data inputted into the location which can hold the output data of the scanning flip-flop concerned with

the directions from the outside is arranged. Since conflict of the logical value in the data output terminal of a scanning flip-flop is canceled by this and failure in generation of an initial pattern and a transition pattern can be prevented, high fault coverage can be obtained. Moreover, since this value maintenance component is arranged only in the part from which conflict is actually started, it can raise fault coverage by the slight increment in hardware.

[0013] Here, as for invention of claim 3, the 4th processing in the inspection easy-ized design approach of the path delay failure concerning invention of said claim 2 shall be equipped with the processing by which D latch's enabling input terminal which has stationed D latch in said integrated circuit, and has been arranged is connected to the external input terminal of said integrated circuit as said value maintenance component.

[0014] Moreover, as for invention of claim 4, the 4th processing in the inspection easy-ized design approach of the path delay failure concerning invention of said claim 2 shall be equipped with the processing by which the enabling input terminal of the tri-state component which has arranged the tri-state component in said integrated circuit, and has been arranged is connected to the external input terminal of said integrated circuit as said value maintenance component.

[0015] Furthermore, as for invention of claim 5, the 4th processing in the inspection easy-ized design approach of the path delay failure concerning invention of said claim 2 shall be equipped with the processing by which the scanning flip-flop or D flip-flop which has arranged the scanning flip-flop or the D flip-flop in said integrated circuit, and has been arranged is connected to the scanning chain already constituted in said integrated circuit as said value maintenance component.

[0016] According to invention of claim 5, it is not necessary to newly add an external terminal to an integrated circuit. Moreover, the inspection easycircuit in can generate an inspection sequence by the same approach as usual.

[0017] And the 4th processing in the inspection easy-ized design approach of path delay failure of said claim 5 in invention of claim 6 In said initial pattern and a transition pattern In the location which can hold the output data of the scanning flip-flop which has the data output terminal to which the logical value to which both logical values were set up and set is contradictory with an initial pattern and a transition pattern, and the output data of said scanning flip-flop, as said value maintenance component It shall have the processing which arranges the selector which carries out the selection output of either of the output data of the arranged scanning flip-flop or a D flip-flop in said integrated circuit.

[0018] As opposed to the integrated circuit with which the inspection easy-ized design according [the solution means which invention of claim 7 provided] to the inspection easy-ized design approach of path delay failure according to claim 3 was performed As an inspection sequence generation method which generates the inspection sequence for detecting the existence of the path delay failure in the signal path of arbitration If the signal outputted from the starting point of a signal path starts, the signal outputted from the starting point of a signal path falls, it starts, path delay failure which is a signal is considered as delay failure and the path delay failure which is a signal is [it falls and] delay failure In D latch stationed by the inspection easy-ized design, one side is connected to the output terminal of the scanning flip-flop connected in said D latch's data input terminal between two data input terminals. By changing into the selector by which another side was connected to the fictitious external input terminal, and connecting the selection-signal input terminal of each selector to a fictitious selection-signal external input terminal further As opposed to the circuit model generated by the 1st processing which generates the circuit model for inspection sequence generation, and said 1st processing While setting a logical value "0" as the starting point of a signal path when the path delay failure for inspection sequence generation started, and this path delay failure was assumed when it was delay failure So that a logical value "1" may be set as the starting point of said signal path when it is falling delay failure, and said signal path may be activated further By setting a logical value as external input terminals other than the starting point of said signal path, or the output terminal of a scanning flip-flop By the path delay failure for [said] inspection sequence generation starting to the circuit model generated by the 2nd processing which generates an initial pattern, and said 1st processing, when it is delay failure While setting a logical value "1" as the starting point of said signal path, when it is falling delay failure, a

logical value "0" is set as the starting point of said signal path. When the starting point of said signal path is the data output terminal of a scanning flip-flop A logical value is set as an external input terminal or the data output terminal of a scanning flip-flop so that it may be in agreement with the logical value to which the input data in the normal mode of this scanning flip-flop was set. Furthermore, so that it may be respectively in agreement with the logical value to which the input data in the normal mode of scanning flip-flops other than the starting point of said signal path when the logical value was set as the data output terminal in said initial pattern was set in said initial pattern By setting a logical value as an external input terminal or the data output terminal of a scanning flip-flop The 3rd processing which generates a transition pattern, and the logical value in the fictitious external input terminal to which the data input terminal of each selector in said circuit model was connected to said integrated circuit It is set as the data output terminal of the scanning flip-flop to which another data input terminal of each selector was connected. Furthermore, the logical value in the external input terminal to which the enabling input terminal of D latch stationed by said inspection easy-ized design was connected The 4th processing which generates the scanning in pattern set up so that said D latch may become data through mode, The logical value set up in said initial pattern and the transition pattern is respectively set as the data output terminal of each scanning flip-flop to said integrated circuit. Furthermore, it considers as a configuration equipped with the 5th processing which generates the scanning in pattern which sets up the logical value of the external input terminal to which said D latch's enabling input terminal was connected so that said D latch may become data-hold mode.

[0019] The inspection sequence for path delay failure is easily generable by considering that D latch stationed by invention of claim 7 to the integrated circuit with which the inspection easy-ized design by the inspection easy-ized design approach according to claim 3 was performed is a selector.

[0020] As opposed to the integrated circuit with which the inspection easy-ized design according [the solution means which invention of claim 8 provided] to the inspection easy-ized design approach of path delay failure according to claim 4 was performed As an inspection sequence generation method of the path delay failure which generates the inspection sequence for detecting the existence of the path delay failure in the signal path of arbitration If the signal outputted from the starting point of a signal path starts, the signal outputted from the starting point of a signal path falls, it starts, path delay failure which is a signal is considered as delay failure and the path delay failure which is a signal is [it falls and] delay failure In the tri-state component arranged by the inspection easy-ized design, one side is connected to the output terminal of the scanning flip-flop connected in the data input terminal of said tri-state component between two data input terminals. By changing into the selector by which another side was connected to the fictitious external input terminal, and connecting the selection-signal input terminal of each selector to a fictitious selection-signal external input terminal further As opposed to the circuit model generated by the 1st processing which generates the circuit model for inspection sequence generation, and said 1st processing By the path delay failure for inspection sequence generation starting, when it is delay failure So that a logical value "1" may be set as the starting point of said signal path when it is falling delay failure and said signal path may be activated further, while setting a logical value "0" as the starting point of said signal path By setting a logical value as external input terminals other than said signal path, or the output terminal of a scanning flip-flop By the path delay failure for [said] inspection sequence generation starting to the circuit model generated by the 2nd processing which generates an initial pattern, and said 1st processing, when it is delay failure While setting a logical value "1" as the starting point of said signal path, when it is falling delay failure, a logical value "0" is set as the starting point of said signal path. When the starting point of said signal path is the data output terminal of a scanning flip-flop A logical value is set as an external input terminal or the data output terminal of a scanning flip-flop so that it may be in agreement with the logical value to which the input data in the normal mode of this scanning flip-flop was set. Furthermore, so that it may be respectively in agreement with the logical value to which the input data in the normal mode of scanning flip-flops other than the starting point of said signal path when the logical value was set as the data output terminal in said initial pattern was set in said initial pattern By setting a logical value as an external input terminal or the data output terminal of a scanning flip-flop The 3rd processing which generates a transition

pattern, and the logical value in the fictitious external input terminal to which the data input terminal of each selector in said circuit model was connected to said integrated circuit It is set as the data output terminal of the scanning flip-flop to which another data input terminal of each selector was connected. Furthermore, the logical value in the external input terminal to which the enabling input terminal of the tri-state component arranged by said inspection easy-ized design was connected The 4th processing which generates the scanning in pattern set up so that said tri-state component may become data through mode, The logical value set up in said initial pattern and the transition pattern is respectively set as the data output terminal of each scanning flip-flop to said integrated circuit. Furthermore, it considers as a configuration equipped with the 5th processing which generates the scanning in pattern which sets up the logical value of the external input terminal to which the enabling input terminal of said tri-state component was connected so that said tri-state component may become data-hold mode.

[0021] The inspection sequence for path delay failure is easily generable by considering that the tri-state component arranged by invention of claim 8 to the integrated circuit with which the inspection easy-ized design by the inspection easy-ized design approach of path delay failure according to claim 4 was performed is a selector.

[0022] The solution means which invention of claim 9 provided has the scanning flip-flop to which the logical value which the logical value was set up and set [in / both / the initial pattern and transition pattern which were generated for inspection of the existence of path delay failure] up is contradictory with an initial pattern and a transition pattern. The value maintenance component which has the function to once hold the inputted data according to the directions from the outside as an integrated circuit by which the design change was carried out so that inspection of the existence of path delay failure might become easy is arranged in the location which can hold the output data of said scanning flip-flop.

[0023] Here, in invention of claim 10, the value maintenance component arranged at the integrated circuit concerning invention of said claim 9 shall be D latch by whom the enabling input terminal was connected to the external input terminal.

[0024] Moreover, in invention of claim 11, the value maintenance component arranged at the integrated circuit concerning invention of said claim 9 shall be a tri-state component by which the enabling input terminal was connected to the external input terminal.

[0025] Furthermore, in invention of claim 12, the value maintenance component arranged at the integrated circuit concerning invention of said claim 9 shall be the scanning flip-flop connected to the scanning chain already constituted before the design change, or a D flip-flop. And in invention of claim 13, the selector which carries out the selection output of either of the output data of the scanning flip-flop arranged as the output data and said value maintenance component of said scanning flip-flop or a D flip-flop shall have been arranged to the integrated circuit concerning invention of said claim 12.

[0026]

[Embodiment of the Invention]

(1st operation gestalt) The 1st operation gestalt of this invention is related with the inspection easy-ized design approach of changing the design of an integrated circuit so that inspection of path delay failure may become easy. Here, the thing of failure which takes [after / while path delay failure makes the starting point an external input terminal or the data output terminal of a scanning flip-flop, / a signal is outputted from the starting point in the signal path which made the terminal point the external output terminal or the data input terminal in the normal mode of a scanning flip-flop, and was constituted from the starting point by only the combinational circuit to the terminal point] the time amount more than a clock period to arrive at a terminal point is said. Moreover, the signal outputted from the starting point starts, when it is a signal, it starts and the path delay failure is called delay failure, by the signal outputted from the starting point falling, when it is a signal, it falls, and it is called delay failure.

[0027] Drawing 1 is a flow chart which shows the flow of the processing in the inspection easy-ized design approach concerning this operation gestalt.

[0028] First, in step S11, it judges whether there is any path delay failure which is not processed yet to the given integrated circuit. Processing is ended when there is no path delay failure which is not processed by progressing to step S12, after choosing one target path delay failure, when there is path

delay failure which is not processed.
[0029] Next, an initial pattern is generated in step S12. The path delay failure specifically chosen as the external input terminal which is the starting point of a signal path, or the data output terminal of a scanning flip-flop starts, when it is delay failure, a logical value "0" is set up, the selected path delay failure falls, and when it is delay failure, a logical value "1" is set up. Furthermore, a logical value by which this signal path is activated is set as other external input terminals or the data output terminal of a scanning flip-flop.
[0030] Next, in step S13, the logical value of each scanning flip-flop with which the logical value was set as the data output terminal in the initial pattern generated at step S12 is memorized.
[0031] Next, a transition pattern is generated in step S14. When it is delay failure, a logical value "1" is set as the starting point of a path, the selected path delay failure specifically starts, the selected path delay failure falls, and when it is delay failure, a logical value "0" is set as the starting point of a path. Moreover, when the starting point of a signal path is the data output terminal of a scanning flip-flop, the input data in the normal mode of this scanning flip-flop sets up other external input terminals or the logical value of a scanning flip-flop so that it may be in agreement with the set-up logical value. Furthermore, the value of an external input terminal or a scanning flip-flop is determined so that it may be respectively in agreement with the logical value which the logical value was set as the data output terminal in the initial pattern generated at step S12, and the data input in the normal mode of the scanning flip-flop this whose data output terminal is not the starting point of a path memorized at step S13.
[0032] Next, in step S15, it judges whether the scanning flip-flop with which the logical value memorized at step S13 and the logical value set as the data output terminal at step S14 are contradictory exists in the given integrated circuit. If the signal line followed when the scanning flip-flop with which a logical value is contradictory existed and a logical value was set as the output terminal of this scanning flip-flop at step S14 does not include path delay failure, it progresses to step S16, and when other, processing of the selected path delay failure returns to step S11 as what was ended.
[0033] Next, in step S16, D latch is inserted in the location which can hold the output data of this scanning flip-flop on the signal line followed when a logical value was set as the output terminal of this scanning flip-flop at step S14 to the scanning flip-flop with which a logical value is contradictory. Moreover, D latch's enabling input terminal is connected to the external input terminal which has already been prepared in the newly added external input terminal or the given integrated circuit and which switches scanning mode and the normal mode. If D latch is inserted, processing of the selected path delay failure will return to step S11 as what was ended.
[0034] The case where it is aimed at an easy circuit is taken for an example, and the inspection easy-ized design approach concerning this operation gestalt is further explained to a detail. Drawing 2 is the circuit diagram showing the integrated circuit set as the object of the inspection easy-ized design approach concerning this operation gestalt. For the NOR gate and 12, as for an inverter and 14, in drawing 2 , the AND gate and 13 are [10a-10g / a scanning flip-flop and 11 / the AND gate and 15] the OR gates.
[0035] In step S11, failure of a processing object is first chosen from the path delay failures which are not processed yet to the integrated circuit shown in drawing 2 . Here, the path delay failure assumed by signal paths 20a, 20b, and 20c shall be chosen. Moreover, the selected path delay failure shall start and shall be delay failure.
[0036] Next, an initial pattern is generated in step S12. First, a logical value "0" is set as the scanning flip-flop 10d data output terminal which the selected path delay failure starts, and serves as the starting point of signal paths 20a, 20b, and 20c since it is delay failure. Furthermore, in order to activate signal path 20b, a logical value "1" is set as scanning flip-flop 10e, and in order to activate signal path 20c, a logical value "0" is set as scanning flip-flop 10f. Drawing 3 is drawing showing the initial pattern generated in step S12.
[0037] Next, in step S13, the logical value "0" set as the scanning flip-flop 10d data output terminal, the logical value "1" set as the data output terminal of scanning flip-flop 10e, and the logical value "0" set as the scanning flip-flop 10f data output terminal are respectively memorized to each scanning flip-flop.

[0038] Next, a transition pattern is generated in step S14. First, a logical value "1" is set as the scanning flip-flop 10d data output terminal which the selected path delay failure starts, and serves as the starting point of signal paths 20a, 20b, and 20c since it is delay failure. Moreover, a logical value "0" is respectively set as the data output terminal of the scanning flip-flops 10a and 10e so that the input data in the this scanning flip-flop 10d normal mode may become a logical value "1." Furthermore, a logical value "1" is respectively set as a scanning flip-flops [10b and 10f] data output terminal so that the logical value "1" set as the data output terminal of scanning flip-flop 10e in the initial pattern generated at step S12 may be given as input data in the normal mode of scanning flip-flop 10e. Moreover, a logical value "1" is set as the data output terminal of scanning flip-flop 10c so that the logical value "0" set as the scanning flip-flop 10f data output terminal in the initial pattern generated at step S12 may be given as input data in the scanning flip-flop 10f normal mode.
[0039] Drawing 4 is drawing showing the transition pattern generated at step S14. In drawing 4 , the logical value to which the figure enclosed with O was set in the initial pattern, and the figure which has not surrounded by O are the logical values set up in the transition pattern.
[0040] Next, in step S15, the scanning flip-flop to which a logical value is contradictory with an initial pattern and a transition pattern is looked for. In drawing 4 , it turns out that the scanning flip-flops [10e and 10f] logical value is contradictory. Moreover, path delay failure shall not be assumed by the signal line from the data output terminal of flip-flop 10e to the input terminal of the NOR gate 11, and the signal line from a flip-flop 10f data output terminal to the input terminal of the AND gate 12.
[0041] Next, D latch is inserted in the output-signal line which are the scanning flip-flops 10e and 10f with which a logical value is contradictory in step S16. Drawing 5 is the circuit diagram showing the result in which D latch was inserted at step S16. In drawing 5 , D latch 30a is inserted between the input terminals of the NOR gate 11 on the signal line followed when generating the data output terminal and transition pattern of scanning flip-flop 10e. Moreover, D latch 30b is inserted between the input terminals of the AND gate 12 on the signal line followed when generating scanning flip-flop 10f a data output terminal and a transition pattern. Furthermore, the newly added external input terminal 31 is connected to the D latches' 30a and 30b inserted enabling input terminal.
[0042] As explained above, according to the inspection easy-ized design approach concerning this operation gestalt, conflict of a logical value is canceled by inserting D latch in the output-signal line of the scanning flip-flop to which the logical value in a data output terminal is contradictory with an initial pattern and a transition pattern. Thereby, in the former, an inspection sequence can be generated now also to the path delay failure which had failed in generation of an inspection sequence, and inspection easy-ization of an integrated circuit is realized. And since D latch is only inserted in the part to which a logical value is contradictory, inspection easy-ization of an integrated circuit can be performed in the amount of hardware smaller than before.
[0043] In addition, a tri-state component may be used instead of D latch. In this case, what is necessary is just to connect the enabling input terminal of the arranged tri-state component to the external input terminal of an integrated circuit.
[0044] (2nd operation gestalt) The 2nd operation gestalt of this invention is also related with the inspection easy-ized design approach of path delay failure. Differing from the 1st operation gestalt is the point that it is not D latch but the flip-flop which is inserted in the part to which a logical value is contradictory.
[0045] Drawing 6 is a flow chart which shows the flow of the processing in the inspection easy-ized design approach concerning this operation gestalt. Steps S21-S25 are the same processings as steps S11-S15 shown in drawing 1 .
[0046] First, in step S21, it judges whether there is any path delay failure which is not processed yet to the given integrated circuit. Processing is ended when there is no path delay failure which is not processed by choosing one target path delay failure and progressing to step S22 when there is path delay failure which is not processed.
[0047] Next, an initial pattern is generated in step S22. The path delay failure specifically chosen as the external input terminal which is the starting point of a signal path, or the data output terminal of a

scanning flip-flop starts, when it is delay failure, a logical value "0" is set up, the selected path delay failure falls, and when it is delay failure, a logical value "1" is set up. Furthermore, a logical value by which this signal path is activated is set as other external input terminals or the data output terminal of a scanning flip-flop.

[0048] Next, in step S23, the logical value of each scanning flip-flop with which the logical value was set as the data output terminal in the initial pattern generated at step S22 is memorized.

[0049] Next, a transition pattern is generated in step S24. When it is delay failure, a logical value "1" is set as the starting point of a path, the selected path delay failure specifically starts, the selected path delay failure falls, and when it is delay failure, a logical value "0" is set as the starting point of a path. Moreover, when the starting point of a signal path is the data output terminal of a scanning flip-flop, other external input terminals or the logical value of a scanning flip-flop is set up so that it may be in agreement with the logical value which the input data in the normal mode of this scanning flip-flop set up. Furthermore, the value of an external input terminal or a scanning flip-flop is determined so that it may be respectively in agreement with the logical value which the logical value was set as the data output terminal in the initial pattern generated at step S22, and the data input in the normal mode of the scanning flip-flop this whose data output terminal is not the starting point of a path memorized at step S23.

[0050] Next, in step S25, it judges whether the scanning flip-flop with which the logical value memorized at step S23 and the logical value set as the data output terminal at step S24 are contradictory exists in the given integrated circuit. If the signal line followed when the scanning flip-flop with which a logical value is contradictory existed and a logical value was set as the output terminal of this scanning flip-flop at step S24 does not include path delay failure, it progresses to step S26, and when other, processing of the selected path delay failure returns to step S21 as what was ended.

[0051] Next, in step S26, a D flip-flop or a scanning flip-flop is inserted in the location which can hold the output data of this scanning flip-flop on the signal line followed when a logical value was set as the output terminal of this scanning flip-flop at step S24 to the scanning flip-flop with which a logical value is contradictory. Moreover, the inserted D flip-flop or the inserted scanning flip-flop is connected to the scanning chain already constituted in the given integrated circuit. If a D flip-flop or a scanning flip-flop is inserted, processing of the selected path delay failure will return to step S21 as what was ended.

[0052] The case where it is aimed at the circuit shown in drawing 2 is taken for an example, and the inspection easy-ized design approach concerning this operation gestalt is further explained to a detail. The initial pattern and transition pattern to signal paths 20a, 20b, and 20c are generated by steps S21-S25, and as shown in drawing 4 , the scanning flip-flops 10e and 10f with which a logical value is contradictory are determined. So far, it is the same as that of the 1st operation gestalt.

[0053] Next, a scanning flip-flop is inserted in the output signal line which are the scanning flip-flops 10e and 10f with which a logical value is contradictory in step S26.

[0054] Drawing 7 is the circuit diagram showing the result in which the scanning flip-flop was inserted at step S26. In drawing 7 , scanning flip-flop 40a is inserted between the input terminals of the NOR gate 11 on the signal line followed when generating the data output terminal and transition pattern of scanning flip-flop 10e. And selector 41a is inserted between scanning flip-flop 40a and the NOR gate 11, and selector 41a carries out a selection output according to the signal inputted from the external input pin 42 to which either the output data of scanning flip-flop 10e and the inserted output data of scanning flip-flop 40a were newly added. Moreover, scanning flip-flop 40b is inserted between the input terminals of the AND gate 12 on the signal line followed when generating scanning flip-flop 10f a data output terminal and a transition pattern. And selector 41b is inserted between scanning flip-flop 40b and the AND gate 12, and selector 41b carries out a selection output according to the signal into which either scanning flip-flop 10f output data and the inserted output data of scanning flip-flop 40b are inputted from said external input pin 42. Furthermore, the inserted scanning flip-flops 40a and 40b are newly connected to the scanning chain constituted by other scanning flip-flops 10a-10g.

[0055] As explained above, according to the inspection easy-ized design approach concerning this operation gestalt, conflict of a logical value is canceled by inserting a D flip-flop or a scanning flip-flop

in the output signal line of the scanning flip-flop to which the logical value in a data output terminal is contradictory with an initial pattern and a transition pattern. Thereby, in the former, an inspection sequence can be generated now also to the path delay failure which had failed in generation of an inspection sequence, and inspection easy-ization of an integrated circuit is realized. And since a D flip-flop or a scanning flip-flop is only inserted in the part to which a logical value is contradictory, inspection easy-ization of an integrated circuit can be performed in the amount of hardware smaller than before.

[0056] Moreover, the circuit by which the design change was carried out by the inspection easy-ized design approach concerning this operation gestalt can generate an inspection sequence with the conventional inspection sequence generation method.

[0057] (3rd operation gestalt) The 3rd operation gestalt of this invention shows the inspection sequence generation method for the integrated circuit to which inspection easy-ization of path delay failure was performed by the inspection easy-ized design approach concerning the 1st operation gestalt.

[0058] Drawing 8 is a flow chart which shows the flow of the processing in the inspection sequence generation method concerning this operation gestalt.

[0059] First, in step S31, the circuit model for inspection sequence generation is generated based on the given integrated circuit. Between two data input terminals, it connects with the scanning flip-flop to which one side was connected in D latch's data input terminal, and, as for another side, D latch specifically stationed by the inspection easy-ized design approach concerning the 1st operation gestalt is changed into the selector of 2 inputs connected to the fictitious external input terminal. moreover, a selection signal with the fictitious selection-signal input terminal of each selector -- business -- it shall connect with an external input terminal

[0060] Next, in step S32, it judges whether there is any path delay failure which is not processed yet to the given integrated circuit. Processing is ended when there is no path delay failure which is not processed by choosing one target path delay failure and progressing to step S33 when there is path delay failure which is not processed.

[0061] In step S33, an initial pattern is generated to the circuit model generated at step S31. A logical value "0" is set as the starting point of a signal path when the selected path delay failure specifically started, and this path delay failure was assumed when it was delay failure, and when it is falling delay failure, a logical value "1" is set as the starting point of a signal path. Moreover, a logical value which activates this signal path is set as other external input terminals and the data output terminal of a scanning flip-flop.

[0062] Next, in step S34, a transition pattern is generated to the circuit model generated at step S31. The selected path delay failure specifically starts, when it is delay failure, a logical value "1" is set as the starting point of a signal path, path delay failure of a processing object falls, and when it is delay failure, a logical value "0" is set up. Moreover, when the starting point of a signal path is the data output terminal of a scanning flip-flop, the input data in the normal mode of this scanning flip-flop sets up other external input terminals or the logical value of a scanning flip-flop so that it may be in agreement with the set-up logical value. Furthermore, the logical value in an external input terminal or the data output terminal of a scanning flip-flop is set up so that it may be respectively in agreement with the logical value to which the logical value was set as the data output terminal in the initial pattern generated at step S33, and the data input in the normal mode of the scanning flip-flop this whose data output terminal is not the starting point of a path was set in the initial pattern.

[0063] Next, in step S35, a scanning in pattern with which the data output terminal of a selector sets the logical value of the data input terminal connected to the fictitious external input terminal between two data input terminals of a selector changed at step S31 as the connected scanning flip-flop is generated to the given integrated circuit. Moreover, in this scanning in pattern, the logical value of the external input terminal connected to D latch's enabling input terminal is set up so that D latch inserted by the inspection easy-ized design may become data through mode.

[0064] Next, in step S36, a scanning in pattern which sets the logical value set up in the transition pattern generated at the initial pattern and step S34 which were generated at step S33 as the data output

terminal of each scanning flip-flop is generated. Moreover, in this scanning in pattern, in order to make into data-hold mode D latch inserted by the inspection easy-ized design, the logical value of the external input terminal connected to D latch's enabling input terminal is set up.
[0065] Next, in step S37, the logical value of the external input terminal which switches scanning mode and the normal mode is set up so that an integrated circuit may become the normal mode, and the inspection pattern (usually pattern) made to generate one clock pulse is generated.
[0066] The case where it is aimed at the circuit shown in drawing 5 is taken for an example, and the inspection sequence generation method concerning this operation gestalt is further explained to a detail. As the 1st operation gestalt explained, as for the circuit shown in drawing 5 , the D latches 30a and 30b are inserted by the inspection easy-ized design.
[0067] First, in step S31, the circuit model for inspection sequence generation is generated based on the circuit shown in drawing 5 . Drawing 9 is the circuit diagram showing the circuit model generated based on the circuit shown in drawing 5 . In drawing 9 , D latch 30a is changed into selector 50a, and D latch 30b is changed into selector 50b. One side is connected to fictitious external input terminal 51a among the data input terminals of selector 50a, and another side is connected to the data output terminal of scanning flip-flop 10e. Moreover, one side is connected to fictitious external input terminal 51b among the data input terminals of selector 50b, and another side is connected to scanning flip-flop 10f. Furthermore, both the selection-signal input terminals of Selectors 50a and 50b are connected to the fictitious selection-signal external input terminal 52.
[0068] Next, in step S32, the standup delay failure in signal paths 20a, 20b, and 20c is chosen among the path delay failures which are not processed yet.
[0069] Next, in step S33, an initial pattern is generated to the circuit model shown in drawing 9 . First, a logical value "0" is set as the scanning flip-flop 10d data output terminal used as the starting point of a signal path when path delay failure was assumed, further, in order to activate Paths 20b and 20c, a logical value "1" is set as the data output terminal of scanning flip-flop 10e, and a logical value "0" is set as scanning flip-flop 10f.
[0070] Next, in step S34, the circuit model shown in drawing 9 is received, and a transition pattern is generated. First, a logical value "1" is set as the scanning flip-flop 10d data output terminal used as the starting point of a signal path. Moreover, in order to give a logical value "1" as input data in the scanning flip-flop 10d normal mode, a logical value "0" is respectively set as the data output terminal of scanning flip-flop 10a, and the data output terminal of selector 50a. At this time, selector 50a shall be directed by the selection signal inputted from the fictitious selection-signal external input terminal 52, and sets a logical value "0" also as fictitious external input terminal 51a so that the data inputted from fictitious external input terminal 51a may always be chosen.
[0071] Moreover, in order to give the logical value "1" set as the data output terminal in the initial pattern as input data in the normal mode of scanning flip-flop 10e, a logical value "1" is respectively set as the data output terminal of scanning flip-flop 10b, and the data output terminal of selector 50b. At this time, selector 50b shall be directed by the selection signal inputted from the fictitious selection-signal external input terminal 52, and sets a logical value "1" also as fictitious external input terminal 51b so that the data inputted from fictitious external input terminal 51b may always be chosen.
[0072] Furthermore, in order to give the logical value "0" set as the data output terminal in the initial pattern as input data in the scanning flip-flop 10f normal mode, a logical value "1" is set as the data output terminal of scanning flip-flop 10c.
[0073] Next, in step S35, a scanning in pattern which sets the logical value "1" which set the logical value "0" set as fictitious external input terminal 51a as the data output terminal of scanning flip-flop 10e to the actual circuit shown in drawing 5 , and was set as fictitious external input terminal 51b as a scanning flip-flop 10f data output terminal is generated. Moreover, in this scanning in pattern, the logical value of the external input terminal 31 is made into the value from which the D latches 30a and 30b become data through mode.
[0074] Next, in step S36, the logical value set as the scanning flip-flops 10a, 10b, 10c, 10d, 10e, and 10f in the initial pattern and the transition pattern, respectively generates a scanning in pattern which is

actually given to each scanning flip-flop to the actual circuit shown in drawing 5 . Moreover, in this scanning in pattern, the logical value of the external input terminal 31 is made into the value from which the D latches 30a and 30b become data-hold mode.

[0075] Next, in step S37, a usual pattern for one clock with which each scanning flip-flop performs the usual shift action is generated. At this time, the logical value of the external input terminal for a mode switch is made into the value from which each scanning flip-flop becomes the normal mode. The inspection sequence over all path delay failures is generated by repeating and performing steps S33-S37 to each path delay failure.

[0076] As explained above, according to the inspection sequence generation method concerning this operation gestalt, an inspection sequence is easily generable to the integrated circuit with which inspection easy-ization was performed by stationing D latch.

[0077] In addition, an inspection sequence is easily generable similarly to the inspection easycircuit in by arranging a tri-state component.

[0078]

[Effect of the Invention] As explained above, according to the inspection easy-ized design approach concerning this invention, inspection of the existence of the path delay failure in an integrated circuit can be made easy by the addition of slight hardware.

[0079] Moreover, according to the inspection sequence generation method concerning this invention, an inspection sequence is easily generable to the integrated circuit formed into inspection easy by the inspection easy-ized design approach concerning this invention. Therefore, the detection ratio of the path delay failure in an integrated circuit can be improved by this invention, without causing the steep increment in an area overhead.

[Translation done.]